CLAIMS

What is claimed is:

1. A graphics processor, comprising:

an arbiter circuit for selecting one of a plurality of inputs in response to a control signal; and

a shader, coupled to the arbiter circuit, operative to process the selected one of the plurality of inputs, the shader including means for performing vertex operations and pixel operations, and performing one of the vertex operations or pixel operations based on the selected one of the plurality of inputs, wherein the shader provides a appearance attribute.

2. The graphics processor of claim 1, further including a vertex storage block for maintaining vertex information.

3. The graphics processor of claim 2, wherein the vertex storage block further includes a parameter cache operative to maintain appearance attribute data for a corresponding vertex and a position cache operative to maintain position data for a corresponding vertex.

4. The graphics processor of claim 1, wherein the appearance attribute is color, and the color is associated with a corresponding pixel when the selected one of the plurality inputs is pixel data.

5. The graphics processor of claim 1, wherein the appearance attribute is position, and the position attribute is associated with a corresponding vertex when the selected one of the plurality of inputs is vertex data.

6. The graphics processor of claim 5, wherein the appearance attribute is color, and the color attribute is associated with a corresponding pixel when the selected one of the plurality of inputs is pixel data.

7. The graphics processor of claim 5, wherein the appearance attribute is one of the following: color, lighting, texture, normal and position data.

8. The graphics processor of claim 1, wherein the appearance value is depth.

9. The graphics processor of claim 1, wherein the selection circuit is a multiplexer, and the control signal is provided by an arbiter, wherein the arbiter is coupled to the multiplexer.

10. The graphics processor of claim 1, wherein the shader provides vertex position data and further including a primitive assembly block, coupled to the shader, operative to generate primitives in response to the vertex position data.

11. The graphics processor of claim 10, further including a raster engine, coupled to the primitive assembly block, operative to generate pixel parameter data in response to the assembled vertex data.

12. The graphics processor of claim 1, wherein the shader generates pixel color information in response to the selected one of the plurality of inputs.

13. The graphics processor of claim 1, wherein the shader includes a register block for maintaining the selected one of the plurality of inputs, a computation element operative to perform arithmetic and logical operations on the data maintained in the register block, and a sequencer for maintaining the instructions that are executed by the computation element.

14. The graphics processor of claim 1, wherein the shader further includes circuitry operative to access a memory.

15. A unified shader, comprising:

a general purpose register block for maintaining data;

a processor unit; and

a sequencer, coupled to the general purpose register block and the processor unit, the sequencer maintaining instructions operative to cause the processor unit to execute vertex calculation and pixel calculation operations on selected data maintained in the general purpose register block.

16. The shader of claim 15, wherein the sequencer further includes circuitry operative to fetch data from a memory.

17. The shader of claim 15, further including a selection circuit operative to provide information to the general purpose block in response to a control signal.

18. The shader of claim 15, wherein the processor unit executes instructions that generate a pixel color in response to the selected one of the plurality of inputs.

19. The shader of claim 15, wherein the processor unit executes vertex calculations while the pixel calculations are still in progress.

20. The shader of claim 15, wherein the processor unit generates vertex position and appearance data in response to a selected one of the plurality of inputs.

21. The shader of claim 17, wherein the selection circuit is a multiplexer and the control signal is provided by an arbiter.